

Energy Efficient Machine-Learning Model Embedded on FPGA for Identification of Sleep Apnea Among Adults

Introduction

This proposed model can monitor and automatically detect sleep apnea with a high degree of precision for adults in a home-based environment. Once apnea is detected, the model will trigger an alarm system that will disturb the user until their breathing is resumed. The proposed system prototype is designed on a field programmable gate-array, (FPGA), on which a feedforward neural network is embedded.

The Importance

Apnea & Its Severity

- Appea is a chronic disorder that is defined by recurrent occurrences of partial or complete cessation of respiration during sleep
- Appea causes a decrease in blood oxygen saturation levels which can contribute to long-term health issues, such as high blood pressure or heart failure

The Alternatives

- Polysomnography is considered the gold standard for diagnosis and monitoring; however, it requires an expensive overnight sleep study
- At-home tests, such as an Ambulatory Polysomnography are portable and cheaper, but are less accurate and still require sleep experts to analyze the results



Electrocardiogram (ECG) Sensor

- Measures electrical activity generated by the heart
- Detects cardiac abnormalities and chest movements

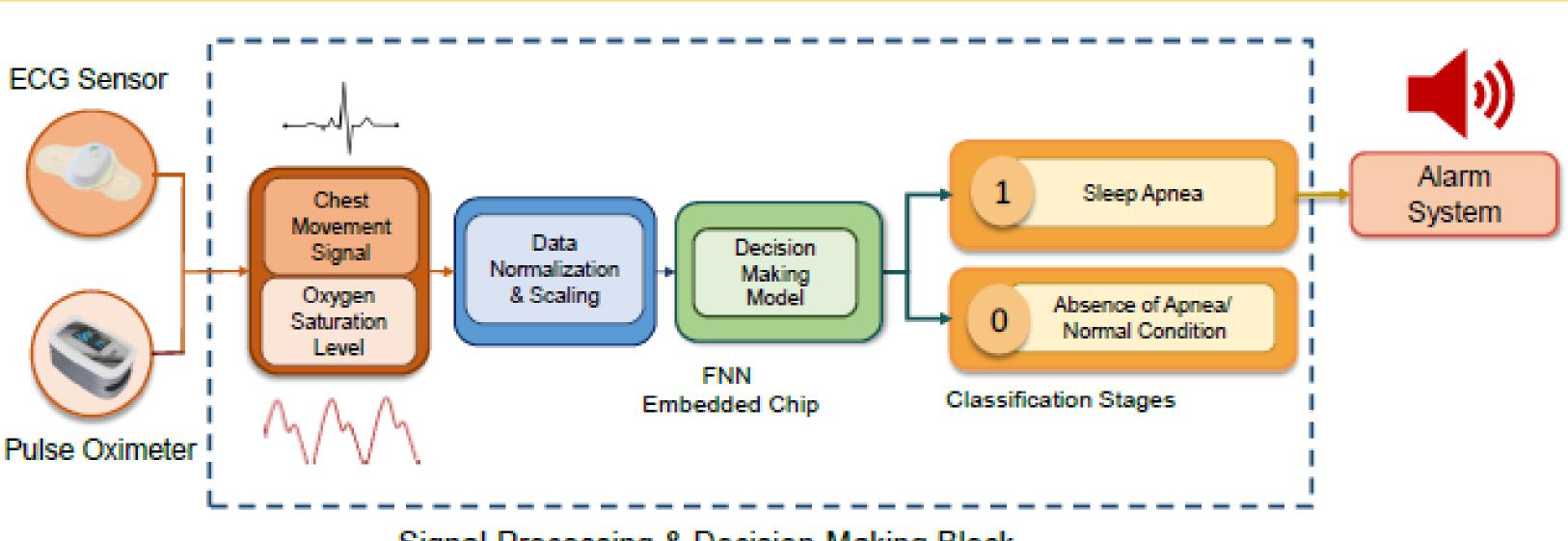
Pulse Oximeter

• Measures blood oxygen saturation levels

Xilinx Vivado

- Software to interface with the embedded design on FPGA
- Programmed using VHDL

System Design



Signal-Processing & Decision-Making Block

Figure 1: Block Diagram of the Overall System Design Using ECG Sensor and Pulse Oximeter as its Input

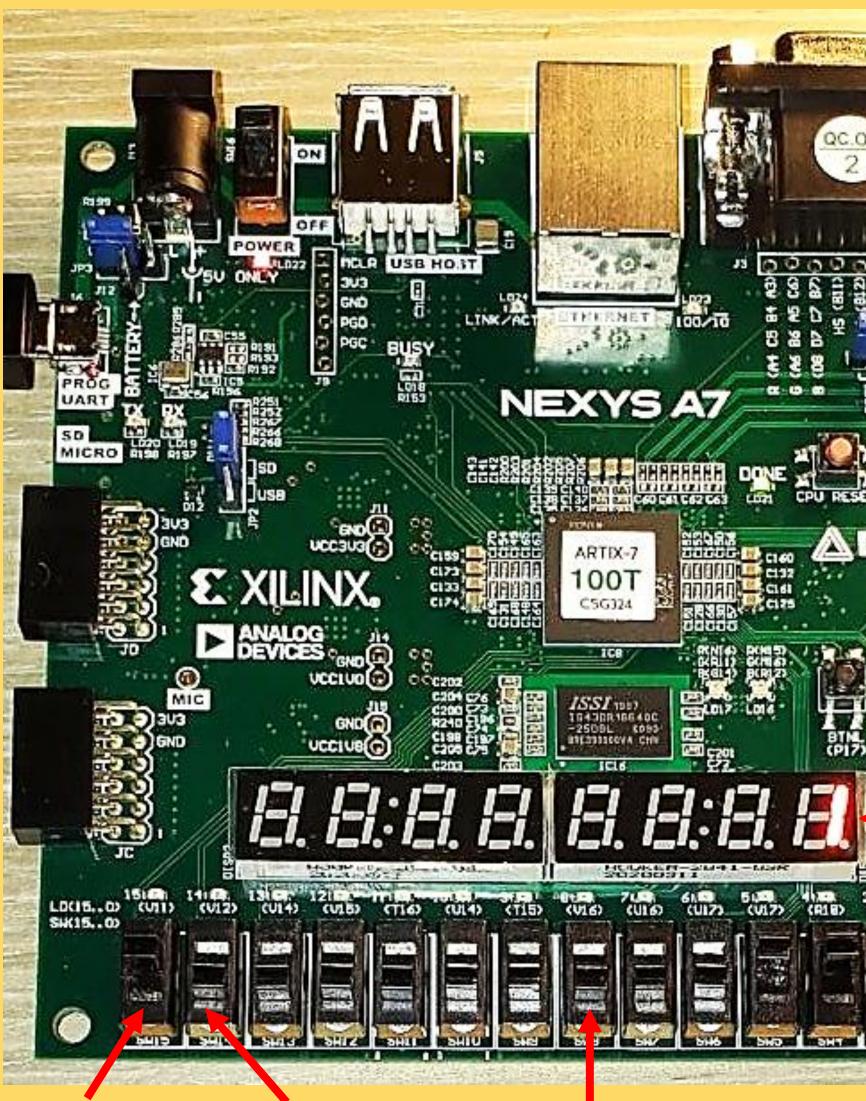
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FPGA Prototype

- Detects apnea with an **88% accuracy** for unseen test data • Takes in two inputs: ECG Sensor and Pulse Oximeter, to feed into neural network
- Most relevant signals for sleep apnea detection [1], [2]
- The inputs are represented by the two leftmost switches \bullet Their data is represented using 9-bit binary numbers, with each bit being represented by a switch, for example, bit 1 corresponds to switch 0
- now show the output of the neural network based on these two inputs
- finally, displaying the output of the network



ECG Sensor Pulse Oximeter Switch 15 Switch 14

Figure 2: FPGA Prototype



Bit 9, Switch 8

[2] Mendonça, F., Mostafa, S.S., Morgado-Dias, F. and Ravelo-García, A.G. (2020). An oximetry based wireless device for sleep apnea detection. Sensors, 20(3), 888. https://doi.org/10.3390/s20030888

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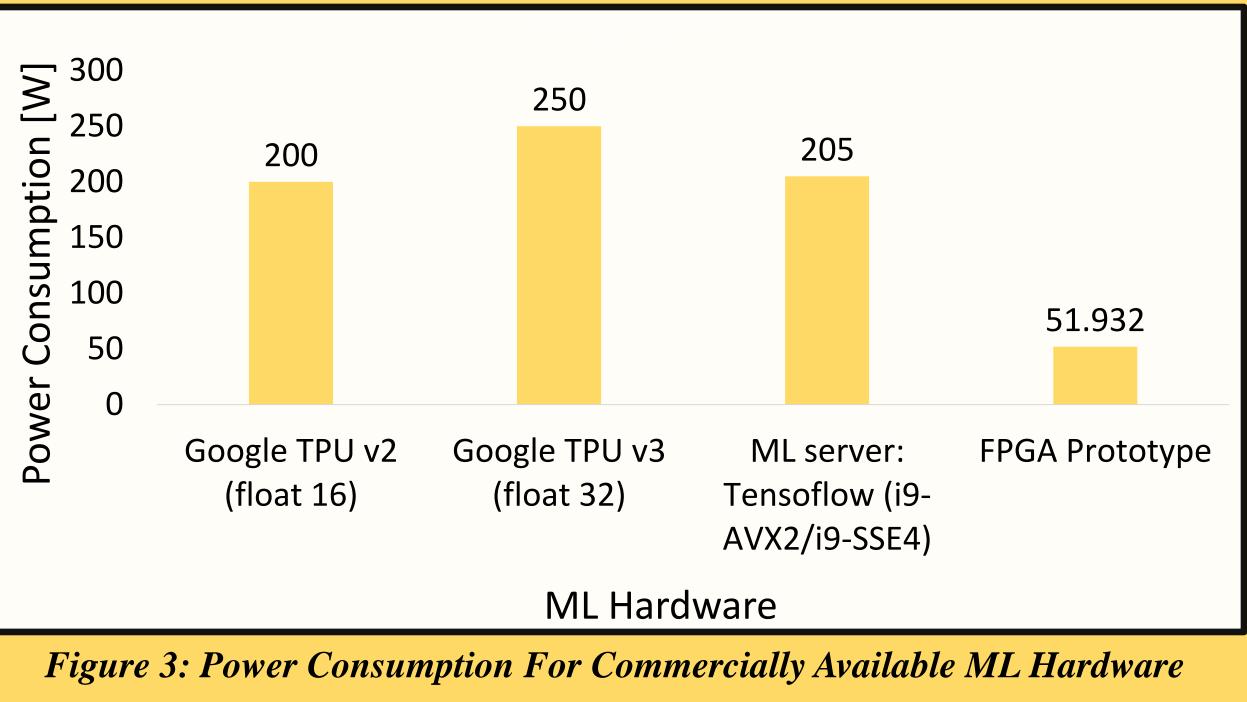
• Figure 2 shows how the model was represented on an Artix-7 Nexys FPGA Board

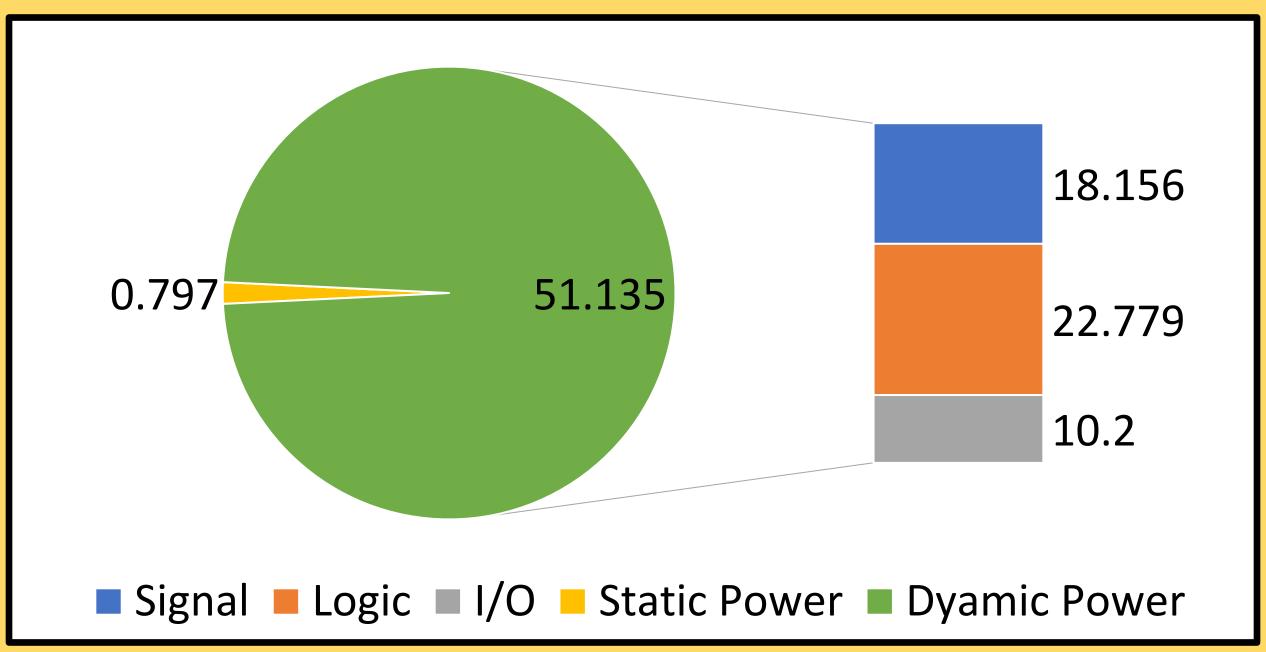
The output is 1 if sleep apnea is occurring and 0 if sleep apnea is not occurring To operate the model, the switch for one of the inputs is flipped and its value, in binary, is entered using the 9 rightmost switches. The Load button is pressed to set the value for that input. This is then repeated for the other input. The display will

This simulates the process of the ECG Sensor and Pulse Oximeter being inputted into the neural network, the network then using these to detect sleep apnea, and

Power Consumption Analysis

- - The prototype consumes **less than a quarter** of the power
 - relative to the commercially available Machine Learning
- accelerators shown in Figure 3
- Figure 4 shows the composition of the 52 watts being consumed • It is split between the following device resource types:







The high accuracy and low power consumption of the proposed system will facilitate its application in sleep apnea monitoring and detection.

Future Applications

Bit 1, Switch 0

• Integration into a system-on-chip, (SOC), platform • Creation of sleep apnea identification devices, such as smart wearable apnea monitoring devices

Load Button

1: sleep apnea

0: normal

References

[1] Ye, G., Yin, H., Chen, T., Chen, H., Cui, L. and Zhang, X. (2021). FENet: A Frequency Extraction Network for Obstructive Sleep Apnea Detection. IEEE Journal of Biomedical and Health Informatics. https://doi.org/10.1109/JBHI.2021.3050113



• This prototype consumes roughly **52 watts**

input/output (I/O), signals, and logic

Figure 4: Power Consumption Report for FPGA Prototype [W]